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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,324	10/10/2001	Giuseppe Rossi	08305-115001 / 20-29	6931

7590 08/24/2004

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EXAMINER	
YAM, STEPHEN K	
ART UNIT	**PAPER NUMBER**
2878	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,324	ROSSI, GIUSEPPE	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 16, 2003 has been entered.

Claim Objections

2. Claims 10, 12, 14, and 16 are objected to because of the following informalities:

In Claim 10, line 1, "associated" should be replaced with "associating".

In Claim 10, line 2, "transconductance settings" should be replaced with "transconductance setting".

In Claim 12, line 3, "o" should be replaced with "of".

In Claim 14, line 3, "a" should be placed before "first bias current".

In Claim 14, line 8, "second current" lacks proper antecedent basis.

In Claim 16, line 1, "the bias selector" lacks proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venes US Patent No. 5,668,501 in view of Mathur et al. US Patent No. 6,661,457.

Claims 1-4, 8, 10, 11, and 13-26

Regarding Claim 1, Venes teaches (see Fig. 4 and 5) a method of controlling gain comprising changing (see Col. 1, lines 62-64) the gain of an amplifier in a gain stage in response to a signal (in (1)) (see Fig. 5), wherein said gain stage is in an output path to an analog to digital converter (30) for readout (see Fig. 5), and changing the power consumption of the amplifier in the gain stage in response to changing the gain (see Col. 6, lines 30-36). Regarding Claim 2, Venes teaches changing the power consumption comprising changing a transconductance (see Col. 4, lines 35-51) of an input transistor (T6, T10) in the amplifier (see Col. 6, lines 18-21). Regarding Claim 3, Venes teaches said changing the power consumption comprising decreasing the power consumption in response to a decrease in the gain, and increasing the power consumption in response to an increase in the gain (see Col. 6, lines 30-36). Regarding Claim 4, Venes teaches associating a plurality of power consumption settings with a plurality of gain settings, selecting a gain setting from said plurality of gain settings, and selecting a power consumption setting associated with the selected gain setting (see Col. 4, lines 40-47 and Col. 6, lines 30-41). Regarding Claim 8, Venes teaches (see Fig. 4 and 5) a method of controlling gain comprising selecting one of a plurality of gain settings (see Col. 1, lines 62-64 and Col. 2, lines 1-11) in response to a signal (on (1)), generating two or more bias currents (see Col. 2, lines 45-53) having bias current values associated with the selected gain setting (see Col. 2, lines 52-53), and

applying said two or more bias currents to a plurality of parallel transistors (T6, $T6_1$,..., $T6_N$, T10, $T10_1$, ..., $T10_N$) (see Fig. 1) in an amplifier in a gain stage in order to change the input transconductance of the amplifier (see Col. 4, lines 40-51 and Col. 6, lines 51-58), wherein said gain stage is in an output path to an analog to digital converter (30) for readout (see Fig. 5). Regarding Claim 10, Venes teaches associating an input transconductance setting to each of a plurality of gain settings (see Col. 4, lines 40-51), each input transconductance setting being associated with a given set of bias current values (see Col. 2, lines 45-57). Regarding Claim 11, Venes teaches (see Fig. 4 and 5) an apparatus comprising a gain stage (20), wherein said gain stage is in an output path to an analog to digital converter (30) for readout and said gain stage having a differential amplifier (10) including a gain selector ($S3_1$... $S3_m$) operative to select one of a plurality of gain settings (see Col. 4, lines 40-42) in response to a signal (in (1)) (see Fig. 5), an input transistor (T6, $T6_1$,..., $T6_N$, T10, $T10_1$, ..., $T10_N$) (see Fig. 1) having a variable input transconductance (see Col. 4, lines 40-51), and a transconductance controller (40, $S1_1$... $S1_N$, $S2_1$... $S2_N$) operative to select an input transconductance of the input transistor in response to a selected gain setting (see Col. 6, lines 47-58). Regarding Claim 13, Venes teaches the input transistor comprising a first plurality of parallel transistors (T6, $T6_1$,..., $T6_N$) (see Fig. 1) connected to a first bias current supply (T1, T5) ("first current mirror"- see Col. 3, lines 54-62), and a second plurality of parallel transistors (T10, $T10_1$, ..., $T10_N$) (see Fig. 1) connected to a second bias current supply ("third current mirror"- see Col. 4, lines 5-16). Regarding Claim 14, Venes teaches the transconductance controller comprising a bias current selector (see Col. 6, lines 47-51) operative to select values for a first bias current and a second bias current associated with a selected gain setting, and a bias current generator (generating binary transconductance

control signal- see Col. 6, lines 47-51) operative to generate a first current (control signals for (S1, $S1_1$,..., $S1_N$)) having the selected value for the first bias current value and apply said first current to the first bias current supply and to generate a second current (control signals for (S2, $S2_1$,..., $S2_N$)) having the selected value for the second bias current value and apply the second current to the second bias current supply (see Col. 4, lines 42-45). Regarding Claim 15, Venes teaches each first and second bias current values producing a different input transconductance (see Col. 4, lines 45-51). Regarding Claim 16, Venes teaches the bias current selector including a plurality of switches ($S1_1$... $S1_N$, $S2_1$... $S2_N$) and is operative to select a different set of switches for each of said plurality of gain settings (see Col. 4, lines 40-51). Regarding Claim 17, Venes teaches the bias current selector operative to select a set of current values in response to the switches selected by the gain selector (see Col. 6, lines 51-58). Regarding Claim 18, Venes teaches (see Fig. 4 and 5) a device comprising a gain stage (20) wherein said gain stage is in an output path to an analog to digital converter (30) for readout (see Fig. 5) and said gain stage having a differential amplifier (10) (see Col. 4, lines 19-23) including a gain selector ($S3_1$... $S3_m$) operative to set the differential amplifier to one of a plurality of gain settings in response to a signal, an input transistor (T6, $T6_1$,..., $T6_N$, T10, $T10_1$, ..., $T10_N$) (see Fig. 1) having an input transconductance (see Col. 4, lines 40-51) and including a first plurality of parallel transistors (T6, $T6_1$,..., $T6_N$) (see Fig. 1) connected to a first bias current supply (T1, T5) ("first current mirror"- see Col. 3, lines 54-62) and a second plurality of parallel transistors (T10, $T10_1$, ..., $T10_N$) (see Fig. 1) connected to a second bias current supply ("third current mirror"- see Col. 4, lines 5-16), and a transconductance controller (40, $S1_1$... $S1_N$, $S2_1$... $S2_N$) operative to change the transconductance of the input transistor to match a selected gain setting (see Col. 6, lines 47-

58) by selectively applying different bias currents (see Col. 4, lines 40-51) to at least one of said first and second bias current supplies (see Col. 2, lines 45-53) for different gain settings (see Col. 6, lines 47-58). Regarding Claim 19, Venes teaches transconductance controller comprising a gain decoder (determining (7)) (see Col. 6, lines 47-51) operative to select one or more bias current values in response to a selected gain response from a plurality of bias current values, and a bias generator (outputting (7)) operative to generate and apply said one or more bias current values to at least one of the first and second bias current supplies (see Fig. 1 and 4). Regarding Claim 20, Venes teaches the transconductance controller operative to increase the transconductance of the input transistor in response to an increase in the gain of the differential amplifier and to decrease the transconductance of the input transistor in response to a decrease in the gain of the differential amplifier (see Col. 6, lines 51-58). Regarding Claim 22, Venes teaches (see Fig. 4 and 5) a method of controlling gain comprising changing the gain (see Col. 4, lines 40-42 and Col. 6, lines 45-58) of an amplifier (10) in a gain stage (20) in response to a signal (in (1)), and changing a gain bandwidth (GBW) of the amplifier in the gain state in response to changing the gain (see Col. 6, lines 8-21). Regarding Claim 23, Venes teaches said changing the GBW comprising changing (see Col. 4, lines 40-51) a transconductance of an input transistor (T6, $T6_1$,..., $T6_N$, T10, $T10_1$, ..., $T10_N$) (see Fig. 1) in the amplifier (see Col. 6, lines 8-12). Regarding Claim 24, Venes teaches said changing the GBW comprising decreasing the GBW in response to a decrease in the gain, and increasing the GBW in response to an increase in the gain (see Col. 6, lines 8-21 and 51-58). Regarding Claims 25 and 26, RMS noise is always present within an analog electrical system and occupies all frequencies, so therefore decreasing the operating bandwidth decreases the amount of total RMS noise (from cutting off the noise in

the deleted frequency bandwidth range) (see also Col. 2, lines 5-8) and decreasing the gain also decreases the amplification amount of the RMS noise, hence decreasing the overall RMS noise level, and for the same reasons, increasing the GBW increases the RMS noise. Venes does not teach the gain stage being within a sensor having an active (APS) pixel array having pixels arranged in rows and columns and the signal as a pixel signal read out from the pixel array using a readout circuit. Mathur et al. teach (see Fig. 1, 3, 6) a sensor having an active (APS) pixel array (10) (see Col. 5, lines 38-42) having pixels arranged in rows and columns (see Fig. 2) and a gain stage (82) having an amplifier with a changing gain (see Col. 7, lines 50-53) for a signal read out from the pixel array using a readout circuit (12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the gain stage for a sensor having an active pixel array having pixels arranged in rows and columns and the signal as a pixel signal read out from the pixel array using a readout circuit, as taught by Mathur et al., in the device and method of Venes, to provide improved gain control for pixel signals for optimal signal processing in an image sensor environment.

Regarding Claims 5-7, 9, and 12, Venes in view of Mathur et al. teach the apparatus and method in Claims 4, 9, and 11, according to the appropriate paragraph above. Regarding Claim 9, Venes teaches each input transconductance setting being associated with a given set of bias current values (see Col. 2, lines 45-57). Venes does not teach the gain setting selected from eight gain settings, the power consumption setting selected from three power consumption settings or each of three power consumption settings associated with a different plurality of gain settings, or each of the plurality of gain settings associated with a different one of the plurality of power consumption and input transconductance settings- however, Venes teaches a different number of

power consumption settings (2^N-1 corresponding to the number of S1 and S2 switches- see Col. 5, lines 32-34) from the number of gain settings (M corresponding to the number of S3 switches- see Col. 6, lines 39-41). It is well known in the art to select an appropriate number of settings for a system, to provide sufficient adjustability without requiring excessively complex components, and to coordinate the settings of a system to functionally operate at an optimum level. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide eight gain settings, three power consumption settings, with each of three power consumption settings associated with a different plurality of gain settings and each of the plurality of gain settings associated with a different one of the plurality of power consumption and input transconductance settings, in the apparatus and method of Venes in view of Mathur et al., to provide an appropriate level of adjustability and coordination for system functionality without excessive system complexity.

Response to Arguments

5. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571)272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SY

THANH X. LUU
PATENT EXAMINER